

10/532643

JC20 Rec'd PTO 25 APR 2005
4001-1201

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re application of

Christian SIEMERS

Conf.

Application No. NEW NATIONAL PHASE

Group

Filed April 25, 2005

Examiner

PROGRAMMABLE LOGIC DEVICE

INFORMATION DISCLOSURE STATEMENT
(SUBMISSION CONCURRENT WITH THE
FILING OF A NEW PATENT APPLICATION)

Assistant Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

April 25, 2005

Sir:

Pursuant to 37 C.F.R. §§ 1.97 and 1.98, and in fulfillment of the duty of disclosure under 37 C.F.R. § 1.56, applicant(s) hereby submit(s) an Information Disclosure Statement for consideration by the Examiner.

I. LIST OF PATENTS, PUBLICATIONS OR OTHER INFORMATION

The patents, publications, or other information submitted for consideration by the Office are listed on PTO-1449, attached hereto.

II. COPIES

- ☒ Copies of the U.S. patents or publications are not submitted since the USPTO has waived their submission for applications filed after June 30, 2003.
- ☐ Submitted herewith is a legible copy of (i) each foreign patent; (ii) each publication or that portion which caused it to be listed; and (iii) all other information or that portion which caused it to be listed.
- ☒ This application is a National Phase of a PCT application. Some or all of the documents listed on the PTO-1449 are not enclosed because they were cited in the International Search Report and copies should have been forwarded from the International Search Authority pursuant to the trilateral agreement between the USPTO, EPO and JPO, or they are U.S. patents or U.S. published applications. If copies are needed, please contact the undersigned.

III. CONCISE EXPLANATION OF THE RELEVANCE
(check at least one box)

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a. ☐ **DOCUMENTS IN THE ENGLISH LANGUAGE**

The attached non U.S. patents, non U.S. patent application publications, foreign publications, or other information in the English language do not require a statement of relevancy.

b. ☐ **DOCUMENTS NOT IN THE ENGLISH LANGUAGE**

A concise explanation of the relevance of all patents, publications, or other information listed that is not in the English language is as follows:

c. ☒ **FOREIGN SEARCH REPORT OR ACTION**

An English language version of the search report or action that indicates the degree of relevance found by the foreign office is attached, thereby satisfying the requirement for a concise explanation. See MPEP 609(A)(3).

d. ☐ **OTHER**

The following additional information is provided for the Examiner's consideration.

FEES

This Information Disclosure Statement is being filed concurrently with the filing of a new patent application; therefore, no fee is required.

If The Examiner has any questions concerning this IDS, he/she is requested to contact the undersigned.

Respectfully submitted,

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Enclosures: ☒ Form PTO-1449(s)
☐ Documents
☒ Foreign Search Report
☐ Other: _____

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

 Attorney Docket No.:
4001-1201

 Application No.:
10/532643

 Applicant:
Christian SIEMERS

 Filing Date:
April 25, 2005

Group Art Unit:

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing date (if appropriate)
	2002/143505	10/3/2002	DRUSINSKY			
	4,870,302	9/26/1989	FREEMAN			

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
	WO 00/69072	11/16/2000	INTERNATIONAL				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	SIEMERS C ET AL.; "Reconfigurable computing based on universal configurable blocks-a new approach for supporting performance- and realtime-dominated applications", COMPUTER ARCHITECTURE CONFERENCE, 2000. ACAC 2000. 5 TH AUSTRALASIAN CANBERRA, ACT, AUSTRALIA 31 JAN. -3 FEB. 2000, LOS ALAMITOS, CA, USA, IEEE COMPUT. SOC, US, 31 January 2000 (2000-01-31), pages 82-89, XP010370824 ISBN: 0-7695-0512-0, Paragraphen 4.3 und 4.4, figures 4,5
	SKLYAROV V: "Reconfigurable models of finite state machines and their implementation in FPGAs", JOURNAL OF SYSTEMS ARCHITECTURE, ELSVIER SCIENCE PUBLISHERS BV., AMSTERDAM, NL, vol. 47, no. 14-15, August 2002 92002-08), pages 1043-1064, XP004375020, ISSN: 1383-7621, paragraphen 6 mit 10 figures 8c, 10
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	DEVADAS S ET AL.; "DECOMPOSITION AND FACTORIZATION OF SEQUENTIAL FINITE STATE MACHINES", IEEE TRANSACTIONS ON COMPUTER AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, IEEE INC. NEW YORK, US, vol. 8, no. 11, 1 November 1989 (1989-11-01), pages 1206-1217, XP000126892, ISSN: 0278-0070, the whole document
	P.M. HEYSTERS, J.M. SMIT, B. MOLENKAMP: "Reconfigurable Architecture for Handheld Devices", PROCEEDINGS OF THE 3D PROGRESS WORKSHOP ON EMBEDDED SYSTEMS, 24 October 2002 (2002-10-24), XP002295073 UTRECHT, the whole document
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	TESSIER R ET AL.; "RECONFIGURABLE COMPUTING FOR DIGITAL SIGNAL PROCESSING: A SURVEY", JOURNAL OF VLSI SIGNAL PROCESSING SYSTEMS FOR SIGNAL, IMAGE, AND VIDEO TECHNOLOGY, KLUWER ACADEMIC PUBLISHERS, DORDRECHT, NL, vol. 28 no. ½, May 2001 (2001-05), pages 7-27, XP001116960, ISSN: 0922-5773, pages 21-22; figures 6, 7

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	E. CANTO ET AL.: "A Temporal Bipartitioning Algorithm for Dynamically Reconfigurable FPGAs", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION - VLSI - SYSTEMS, vol. 9, no. 1, February 2001 (2001-02), pages 210-218, XP002295077, the whole document
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EXAMINER:	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.	

* English language abstract provided for the Examiner's convenience

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